A GaAs FET Model for Large-Signal Applications

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Abstract—**The use of GaAs FET's under large-signal conditions requires a knowledge of the nonlinear behavior of these devices. A computer program, based on a circuit model with nonlinear elements, has been developed which provides this information. Results from the computer model and examples of its use in microwave circuit design are given.**

I. INTRODUCTION

THE DESIGN OF power GaAs FET amplifiers, mixers, and oscillators can be accomplished more precisely and easily if the large-signal characteristics of the active devices are known. In general, it has been difficult to obtain accurate large-signal parameters for semiconductor devices, especially at microwave frequencies. Most of the data available for microwave FET's have been obtained experimentally by using some form of active or passive load-pull measurement method or by measuring large-signal S-parameters [1]. Since large-signal S-parameters are an extension of small-signal theory, a linear two-port model is assumed, which is not entirely valid for nonlinear FET operation. Also, S-parameters are defined with constant (usually 50-Ω) terminations for the source and load impedances. Thus, the FET is not measured under actual circuit conditions. The ability to vary the source and load impedances presented to the FET is the main difference and advantage of load-pull techniques over large-signal S-parameter measurements. One of the advantages of large-signal S-parameters is that swept-frequency measurements can easily be made over wide frequency ranges. However, load-pull techniques are difficult to implement and require a significant amount of test time in order to characterize a single device, although the data obtained simulates the in-circuit performance of the FET.

A variety of models have been devised to aid in the understanding of the large-signal behavior of FET's. These models range from the original low-frequency model proposed by Shockley [2], which was valid for long gate-length Si or Ge devices (along with attempts to improve the model by incorporating velocity saturation effects [3]), to numerical solutions that solved the partial differential equations describing the charge transport effects in the FET [4]. These time-domain solutions are inefficient and are not practical for real-time computations. A significant amount of computer time can be saved by approximating the solutions to the semiconductor differential equations [5], but adding the effects of arbitrary input and output networks, which may be characterized by laboratory frequency-domain measurements, are difficult in a time-domain solution. Another, more practical, approach is to attempt an extension of linear circuit theory to include nonlinear elements [6].

In this paper, an efficient frequency-domain solution based on small-signal S-parameters and pulsed $I-V$ measurements will be presented. This work extends the model developed by Willing [7], which was solved in the time-domain, to include the effects of the drain-to-gate breakdown currents and forward gate conduction. Arbitrary input and output networks that can either be represented by measured data or computed by a microwave circuit program, such as SUPER-COMPACT™ [8], are easily included. Thus, an accurate in-circuit FET performance can be computed on-line to complement other interactive analysis methods.

This numerical model also allows the designer to observe the performance variations of the FET as a function of bias voltages, drive level, and terminal impedances. Changes in device characteristics, such as the slice-to-slice variations of g_m, C_{GS}, and breakdown parameters, can also be readily accommodated in the model so that the production performance of the FET can be analyzed on a real-time basis. Since the model is based on physical measurements, no knowledge of device geometry or doping profile is required, and thus any FET can be evaluated using this model.

By combining this dynamic model with the frequency-domain characteristics of the terminating networks, the circuit performance for a typical amplifier, frequency multiplier, or single-gate FET mixer can be analyzed. Since a full frequency-domain analysis is conducted and all the circuit node voltages and loop currents are accessible by the computer program, any desired parameter can be calculated. Quantities, such as voltage waveforms, and performance criteria, such as intermodulation distortion and compression characteristics, which are sometimes difficult to obtain by conventional measurement methods, are easily computed. The effects on circuit gain and power output due to reflected or absorbed harmonic energy by the terminating networks can also be simulated.

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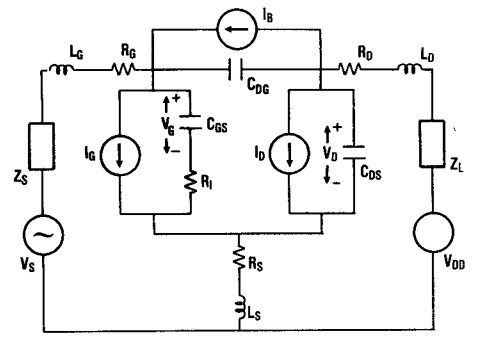


Fig. 1. FET circuit model with source and load impedances.

II. Circuit Model and Nonlinear Elements

At small-signal levels, the behavior of GaAs FET's may be effectively modeled by a circuit with ordinary linear elements, and the circuit model can be retained for large-signal conditions if the proper elements are modified to reflect the nonlinear behavior. In Fig. 1, an equivalent circuit is shown which was used to model the GaAs FET with the input and output matching networks. The circuit model employs both linear and nonlinear elements which are characterized by measurement or modeling.

The values for linear elements in the model are obtained in three ways. First, physical measurements provide the parasitic resistances associated with the FET (R_G, R_D, R_S), and the inductance values associated with bond wire connections (L_G, L_D, L_S) are analytically determined. Second, from a knowledge of the matching circuit topology, an analysis can be performed on CAD programs, such as SUPER-COMPACT™, to provide impedance values (Z_S and Z_L) for the signal and harmonic frequencies of interest. If desired, the impedance information may also be obtained from laboratory S-parameter measurements. Third, a linear model for the FET, consisting of capacitances between the source, gate, and drain (C_{GS}, C_{DS}, C_{DG}), an internal charging resistance (R_I), linear transconductance, output conductance, and a time delay (to model the drain current), is used. The element values in the linear FET model are found by determining model values which will produce the best fit to measured small-signal S-parameter data for the device.

The greatest contribution to the nonlinear behavior of a GaAs FET may be attributed to the variation of the drain current as a function of gate and drain voltages. Since this current is the ultimate source of the power delivered to the output load, it must be expected that deviations from linear behavior in this current will have the largest effect. In addition, at the extremes of positive gate voltage and large positive drain voltage, respectively, the nonlinear forward-bias gate current and gate-to-drain breakdown current flow. The effect in both cases is to limit the current delivered to the load and to clip the output voltage waveform. Thus, these currents will also affect the gain compression at large-signal levels and contribute to the harmonic content in the current and voltage waveforms.

In this model, the nonlinear currents I_D (drain current), I_G (forward-bias gate current), and I_B (gate-to-drain breakdown current), are assumed to be functions of the instantaneous internal gate voltage V_G and drain voltage V_D. This feature allows the use of essentially dc measurements to characterize these currents. Pulsed $I-V$ measurements may be made on the FET to be modeled, and an analysis of this data, along with the values of the linear circuit model elements, allows the calculation of these nonlinear currents.

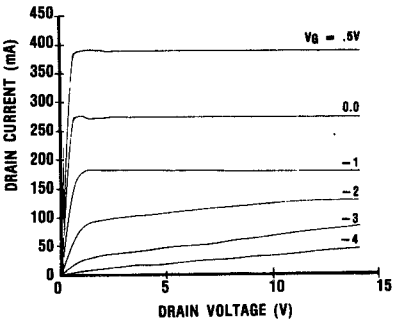


Fig. 2. FET drain current characteristics for a 600-μm FET.

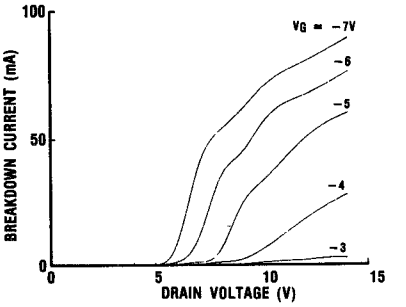


Fig. 3. FET gate-to-drain breakdown current characteristics for a 600-μm FET.

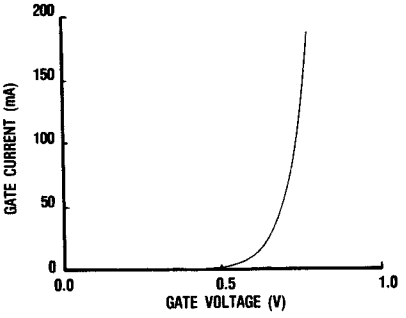


Fig. 4. FET forward-bias gate current for a 600-μm FET.

As an example of the use of the model, we have chosen in this paper to examine the application of the model to a 600-μm$\times$0.7-μm gate power GaAs FET. The drain-current characteristics for this FET are shown in Fig. 2. In Fig. 3, the gate-to-drain breakdown current characteristics for the same FET are shown, and Fig. 4 illustrates the FET's forward-bias gate current, which is assumed dependent on V_G only, and exhibits the typical Schottky-diode current behavior. This information was obtained from 5-μs (gate) and 2-μs (drain) pulsed $I-V$ data. The linear elements for this FET have the values shown in Table I. The input and

TABLE I
600-μm FET LINEAR ELEMENT VALUES

R_G = 1.1Ω	L_G = 0.08 nH
R_S = 1.1Ω	L_S = 0.015 nH
R_D = 1.4Ω	L_D = 0.26 nH
R_I = 2.5Ω	C_{GS} = 1.0 pF
C_{DS} = 0.15 pF	C_{DG} = 0.035 pF

output matching circuits were modeled using SUPER-COMPACT™ to provide their impedance values for the signal and harmonic frequencies investigated.

III. Numerical Solution and Model Verification

An analysis of the circuit of Fig. 1 using Kirchhoff's laws in the frequency-domain results in coupled, complex, simultaneous algebraic equations, with V_G and V_D as the independent variables. For each Fourier component (dc, signal, and harmonics) there are two complex equations

$$AV_G + BV_D = C \tag{1}$$

$$DV_G + EV_D = F \tag{2}$$

where

$$A = 1 + j\omega[(Z_2 + R_I)C_{GS} + (Z_1 + Z_S)(C_{GS} + C_{DG} + j\omega R_I C_{GS} C_{DG})] \tag{3}$$

$$B = j\omega[-(Z_1 + Z_S)C_{DG} + Z_2 C_{DS}] \tag{4}$$

$$C = -(Z_1 + Z_2 + Z_S)I_G + (Z_1 + Z_S)I_B - Z_2 I_D + V_S \tag{5}$$

$$D = j\omega[Z_2 C_{GS} - (Z_3 + Z_L)(j\omega R_I C_{GS} C_{DS} + C_{DS})] \tag{6}$$

$$E = 1 + j\omega[Z_2 C_{DS} + (Z_3 + Z_L)(C_{DG} + C_{GS})] \tag{7}$$

$$F = -Z_2 I_G - (Z_3 + Z_L)I_B - (Z_2 + Z_3 + Z_L)I_D + V_{DD} \tag{8}$$

and

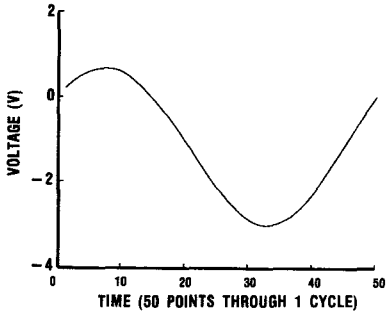
$$Z_1 = R_G + j\omega L_G \tag{9}$$

$$Z_2 = R_S + j\omega L_S \tag{10}$$

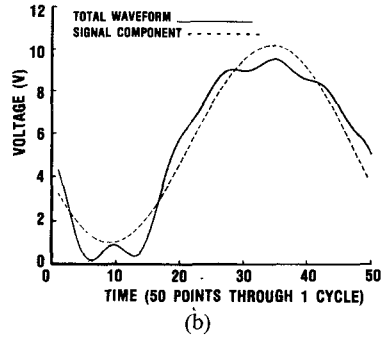
$$Z_3 = R_D + j\omega L_D. \tag{11}$$

The nonlinearity in the equations is contained in the elements I_D, I_B, and I_G, which depend on V_G and V_D. Equations (1) and (2) define V_G and V_D only implicitly because of this fact, and the system is best solved computationally using an iterative technique.

The existence of nonlinear elements in the circuit model in Fig. 1 complicates the circuit analysis, however. The linear elements, R's, L's, and C's as modeled within the FET, are primarily frequency-domain elements. In the time-domain, the expressions for inductance and capacitance are no longer simple algebraic quantities, but must be put in terms of time derivatives and integrals. The same feature is true for the input and output matching networks,



(a)



(b)

Fig. 5. (a) Gate and (b) drain voltage waveforms at 10 GHz and 20-dBm input power.

where time-domain expressions for microwave element circuits may be very difficult to obtain. Conversely, the nonlinear elements are functions of instantaneous voltages, and thus are primarily time-domain elements with no simple expression (even in a nonlinear form) in the frequency-domain. The technique for obtaining a self-consistent solution for the nonlinear circuit must then use Fourier transforms to alternate between the time- and frequency-domains.

It should be noted that the nature of the nonlinear problem required that two common simplifications be avoided in obtaining a solution. First, one may not restrict the solutions of the problem to only the signal frequency [6]. The absence of the higher harmonics in the solution would mean that the RF part of any current must be a simple sinusoid. This would seriously violate the representations of the gate forward-bias and gate-to-drain breakdown currents which must appear as positive, and are nonzero only in a portion of the voltage cycle. The drain current characteristics are also greatly different at the maximum and minimum values of the current under large-signal conditions. Thus, a sufficient number of harmonics must be included in the analysis to adequately represent the time-dependent behavior of the nonlinear elements.

The computed effect of the harmonic content at large-signal levels is indicated in Fig. 5 for the 600-μm FET described earlier at 10 GHz with an input power of 20 dBm. As can be seen, there is considerable harmonic content above the signal level, and this may be important for the designer, depending on the application for which the FET is used. In practice, we have found that the effects of the higher harmonics contribute between -1 dB to $+1$ dB to the signal power, and that the shape of the broad-

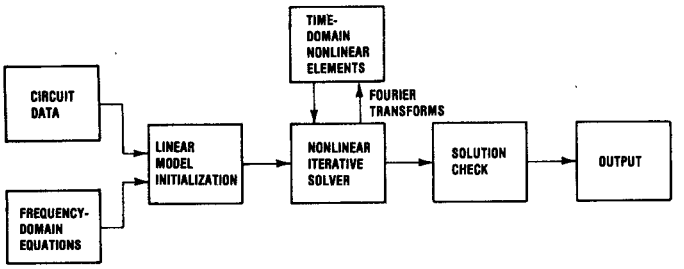


Fig. 6. Large-signal model solution process.

band signal output power versus frequency curve under gain compression is modeled much better when the higher harmonics are included. Typically, harmonics above the fourth do not affect the signal output power significantly. The effect of the higher harmonics is especially important at the low end of the frequency band of interest because of complex terminations; but care must be taken in the interpretation of results at the high frequency end. At 2 GHz, for example, the first three harmonics at 4, 6, and 8 GHz may well lie within the frequency band being used, but at 18 GHz the harmonics at 36, 54, and 72 GHz may be high enough to introduce error due to poor circuit modeling at these frequencies. Nevertheless, the higher harmonics in the analysis cannot be excluded without substantial distortion of the character of the nonlinear elements.

Second, the expression of the nonlinear currents as nonlinear conductances must be avoided. The definition of such fictitious elements by use of the ratio of the Fourier current component to the Fourier voltage component for the fundamental and harmonic frequencies

$$G_n = \frac{I_n}{V_n} \tag{12}$$

is unjustified, because a nonzero Fourier current component need not imply that the corresponding voltage component is nonzero. As an example of this, consider a diode-like element which permits current flow above a certain threshold voltage, with zero current below the threshold. A signal voltage at a single frequency can produce spike-like current flows which have nonzero harmonic content. The definition of conductance is inapplicable at the harmonic levels because of the zero values for the voltage harmonics. In practice, this causes either large computational errors or zero divide checks in the solution procedure.

The solution process is illustrated in Fig. 6. To begin the iterative solution process, an initial approximation to the solution is made by neglecting the gate forward-bias and gate-to-drain currents and assuming a linear conductance value for calculating the drain current. As each iteration is done, a Fourier transform produces the time-domain V_G and V_D functions, and from these functions the nonlinear current functions are generated. A Fourier transform then yields a frequency-domain expression for the nonlinear elements, and the next solution iteration proceeds. Finally, the accuracy of the solution is determined by examining the circuit's current and voltage values for consistency with Kirchhoff's laws.

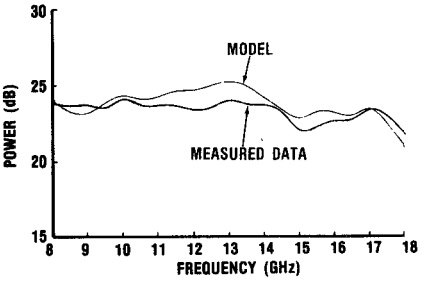


Fig. 7. Measured and computed output power at the 1-dB gain compression point for a 600-μm FET.

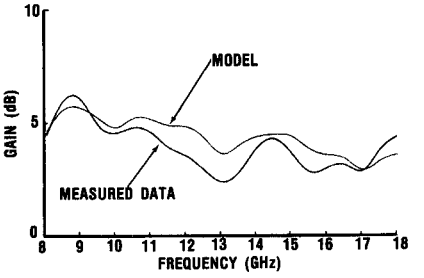


Fig. 8. Measured and computed output gain at the 1-dB gain compression point for a 600-μm FET.

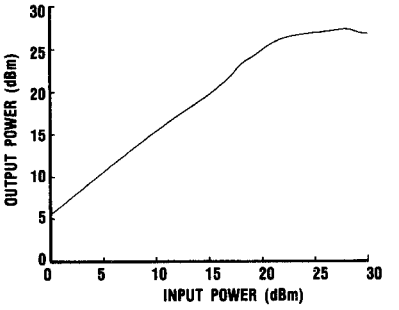


Fig. 9. Computed output versus input power at 10 GHz.

The 600-μm FET (described in the previous section) with input and output matching networks was measured for gain and output power using an automatic network analyzer at the 1-dB gain compression point, and the data was used for comparison with the large-signal model. Fig. 7 shows the measured and predicted output powers in decibels referred to 1 mW for the 1-dB gain compression point of the operating FET in the 8–18-GHz band, and Fig. 8 shows the measured and predicted gain values at the 1-dB gain compression point for the same frequency range. For the comparison shown, three harmonics above the signal frequency have been used in the analysis. The comparisons show a good correlation (less than 0.7-dB average deviation over the band with a maximum of 1.3 dB), and the differences may be at least partially attributed to measurement errors and the fact that some losses (notably radiation loss in the matching circuits) have not been included in the model. In Fig. 9, a plot of computed output versus input power is shown at the 10-GHz frequency, which illustrates the deviation from linearity at high input power levels.

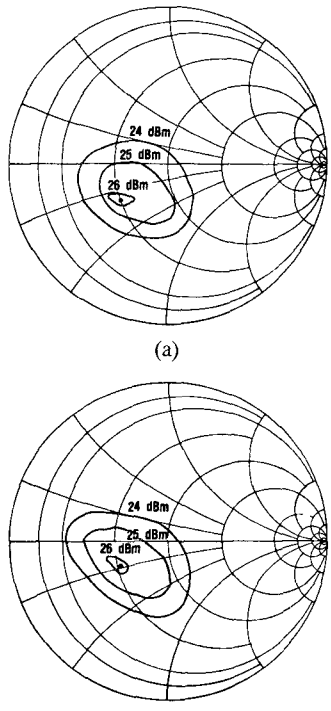


Fig. 10. Constant power contours at 1-dB gain compression at (a) 8 and (b) 16 GHz.

IV. Results and Applications

As mentioned earlier, one of the most difficult parameters to obtain from either load-pull measurements or large-signal S-parameter measurements is the optimum load impedance. Since this impedance is dependent on drive level, dc-bias conditions, and source impedance, an accurate impedance value is difficult to determine from measurement; but, it can be easily determined using the large-signal model. This impedance, which may vary greatly from the conjugate small-signal FET output impedance, is a function of frequency and is the impedance that must be presented to the FET in order to obtain maximum output power. However, it is usually very difficult or impossible to synthesize an output load network that can present the FET with the optimum impedance over very large bandwidths. If constant power and gain contours are calculated for a sufficient number of frequencies throughout the band of interest, an output circuit may be synthesized which optimizes the resulting amplifier's power output and gain performance. The resulting FET and output circuit can now be analyzed so that the required input network for a particular amplifier can be synthesized. The total amplifier performance can then be computed.

Typical constant power contours for the 600-μm power FET for two frequencies are shown in Fig. 10. It should be noted that these contours become smaller with increasing frequency due to the performance degradation of the FET. These contours are also a function of dc bias, drive power, and harmonic terminations. The contours shown in Fig. 10 represent the optimum load impedance for the FET biased at 60 percent of I_{DSS} and driven at the 1-dB gain compression point. With the impedance and gain data available, single or multistage amplifiers can be accurately designed.

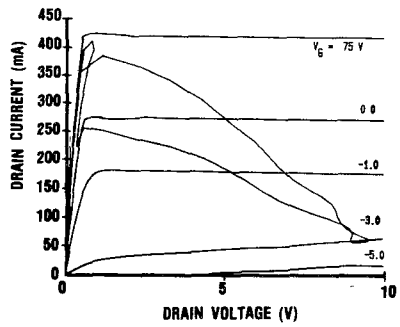


Fig. 11. Dynamic operating path at 20-dBm input power at 10 GHz.

Since all the loop current and node voltages within the circuit model are calculated by the computer program, the gate and drain voltage waveforms as well as the gate–drain transfer characteristics can easily be plotted. The gate and drain waveforms are illustrated in Fig. 5 and the dynamic operating path for the 600-μm FET (at 1-dB gain compression) is shown in Fig. 11. By examining these waveforms, the dc-bias conditions required to establish a particular class of amplifier operation (A, B, etc.), or to maximize the power output, can be determined. In addition, information concerning the harmonic distortion of a typical amplifier can be gained. For instance, if the drive power and operating point are adjusted so that the drain voltage waveform is symmetrically clipped (square wave), the second harmonic output can be minimized. Conversely, if the drive power, operating point and load-line are adjusted so that an RF half-cycle is reproduced at the drain, the resulting amplifier stage can be used in the design of push-pull amplifiers or balanced multipliers. It should be noted that push-pull Class B amplifiers at microwave frequencies are constructed with 180° power dividers or baluns so that a full RF cycle is present at the output port. Somewhat higher values of the load impedances must also be presented to the FET so that reasonable values of power gain are obtained.

Because of the efficiency of the solution technique, the model could be extended to include multiple FET's and their associated input, interstage, and output networks to form multistage models. Composite circuit performance can then be calculated or an optimization technique can adjust the external circuit values to obtain a predescribed amplifier performance.

V. Conclusions

Due to the stringent requirements imposed on modern microwave components, the use of nonlinear modeling to aid in the design of power FET amplifiers, mixers, and oscillators is imperative. The model presented in this work, which was developed from physical measurements, and linear and nonlinear circuit theory, accurately predicts the large-signal behavior of power FET's. Although this solution method is primarily carried out in the frequency-domain, it is efficient and well suited for computer-

aided interactive design and analysis. Because of the frequency-domain treatment, measured or computed *S*-parameter representations of any desired input or output network can be included in the total circuit model. The actual in-circuit performance of any FET may be simulated, thus allowing the designer to better understand the problems of device fabrication and high-volume component manufacturing.

Similar performance information can be obtained from load-pull techniques, but the FET evaluation and dynamic circuit measurements required are time consuming and tedious. Any changes in circuit bias conditions or drive power can only be incorporated in new circuit design by recharacterizing the FET. However, parameters such as intermodulation distortion, optimum load impedances, compression characteristics, harmonic content, and circuit gain at any bias condition can be calculated quickly with the nonlinear model described there. Thus, considerable time and effort can be eliminated in the design of modern microwave components.

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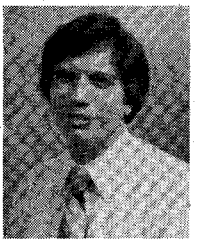

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